UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,769	06/29/2001	Darren L. Abramson	42390.P10573	2024

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EXAMINER
MASON, DONNA K

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	09/896,769	ABRAMSON ET AL.
	Examiner	Art Unit
	Donna K. Mason	2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _08 July 2004_.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-30_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-30_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _10 August 2004_ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Drawings

1.   The drawings are objected to because Figs. 8A, 8B and 8C should be labeled

consistent with the specification, for a better understanding of the drawings. (*See* 37

CFR 1.84(o).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in

reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. The figure or figure

number of an amended drawing should not be labeled as "amended." If a drawing figure

is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for

consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. The replacement sheet(s) should be labeled "Replacement

Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of

the drawing figures. If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The

objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   Claims 1, 11, 21, and 27 are rejected under 35 U.S.C. 102(e) as being

anticipated by U.S. Patent No. 6,763,391 to Ludtke.

With regard to claims 1 and 11, Ludtke discloses a method including removing a

work item from an enabled bus schedule data structure (column 9, lines 17-24) and

generating a coherency signal in response to removing the work item (column 9, lines

35-43)), and reclaiming the work item whenever the coherency signal is generated

(column 9, lines 56-60). Ludtke also discloses a machine-readable medium that

provides instructions, which when executed by a machine, cause the machine to

perform the claimed method (column 9, lines 6-16).

With regard to claims 21 and 27, Ludtke discloses an apparatus and computer

system, the apparatus including: a command register including a command signal bit to

indicate a removal of a work item from an expansion bus schedule data structure

including a plurality of work items (column 9, lines 17-24); a status register including a

status signal bit to notify an expansion bus host controller driver that the work item may

be reclaimed (column 9, lines 56-60); and a microcontroller to process the expansion

bus schedule data structure and to modify the status signal bit of the status register in response to the removal of the work item from the expansion bus schedule data structure (column 9, lines 35-60).

Therefore, Ludtke reads on the invention as specified in claims 1, 11, 21, and 27.

4.   Claims 1, 10, 11, 20, 21, and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,205,501 to Brief, et al. ("Brief").

With regard to claims 1 and 11, Brief discloses a method including: removing a work item of a plurality of work items from an enabled expansion bus schedule data structure (column 8, lines 63-67 to column 9, lines 1-2); generating a coherency signal utilizing an expansion bus host controller in response to removing the work item from the enabled expansion bus schedule data structure (column 5, lines 44-63 and column 9, lines 2-31); and reclaiming the work item whenever the coherency signal is generated (column 9, lines 28-31). Brief also discloses a machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform the claimed method (column 1, lines 28-36).

With regard to claims 10 and 20, Brief discloses a method and machine-readable medium, the method further including storing each of the plurality of work items within a memory, where reclaiming the work item in response to generating the coherency signal comprises freeing a portion of the memory associated with the work item (column 9, lines 28-31).

With regard to claims 21 and 27, Brief discloses an apparatus and computer system, the apparatus including: a command register including a command signal bit to indicate a removal of a work item from an expansion bus schedule data structure including a plurality of work items (column 8, lines 63-67 to column 9, lines 1-5); a status register including a status signal bit to notify an expansion bus host controller driver that the work item may be reclaimed (column 5, lines 44-63 and column 9, lines 2-31); and a microcontroller to process the expansion bus schedule data structure and to modify the status signal bit of the status register in response to the removal of the work item from the expansion bus schedule data structure (column 9, lines 22-31).

Therefore, Brief reads on the invention as specified in claims 1, 10, 11, 20, 21, and 27.

5.   Claims 1, 5-10, 11, 15-20, 21, and 23-30 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,804,762 to Dussud, et al. ("Dussud").

With regard to claims 1 and 11, Dussud discloses a method including: removing a work item of a plurality of work items from an enabled expansion bus schedule data structure (column 8, lines 4-11); generating a coherency signal utilizing an expansion bus host controller in response to removing the work item from the enabled expansion bus schedule data structure (column 9, lines 3-7); and reclaiming the work item whenever the coherency signal is generated (column 9, lines 3-7). Dussud also discloses a machine-readable medium that provides instructions, which when executed

by a machine, cause the machine to perform the claimed method (column 2, lines 36-41). Also, *see generally*, column 4, lines 29-32 and column 5, lines 3-6.

With regard to claims 10 and 20, Dussud discloses a method and machine-readable medium, the method further including storing each of the plurality of work items within a memory, where reclaiming the work item in response to generating the coherency signal comprises freeing a portion of the memory associated with the work item (column 1, lines 33-39).

With regard to claims 21 and 27, Dussud discloses an apparatus and computer system, the apparatus including: a command register including a command signal bit to indicate a removal of a work item from an expansion bus schedule data structure including a plurality of work items (column 8, lines 4-11); a status register including a status signal bit to notify an expansion bus host controller driver that the work item may be reclaimed (column 9, lines 3-7); and a microcontroller to process the expansion bus schedule data structure and to modify the status signal bit of the status register in response to the removal of the work item from the expansion bus schedule data structure (column 9, lines 1-3). Also, *see generally*, column 4, lines 29-32 and column 5, lines 3-6.

With regard to claims 5-9, 15-19, 23-26, and 28-30, Dussud discloses a method and a machine-readable medium, where generating a coherency signal utilizing an expansion bus host controller in response to removing the work item from the enabled expansion bus schedule data structure includes: traversing the plurality of work items according to a sequence; storing a copy of a work item within a memory in response to

traversing the plurality of work items; and generating a coherency signal utilizing the

copy of the work item (*see generally*, column 5, lines 45-65 and column 7, lines 66-67 to

column 9, lines 1-7).

Therefore, Dussud reads on the invention as specified in claims 1, 5-10, 11, 15-

20, 21, and 23-30.

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which the subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

7.   Claims 2-4, 12-14 and 22 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Ludtke in view of *Universal Host Controller Interface (UHCI) Design*

Guide, Revision 1.1 by Intel ("Intel").

As discussed above with regard to the 35 USC 102(e) rejection, Ludtke discloses

all the features of claims 1, 11 and 21.   With regard to claims 4 and 14, Ludtke also

discloses the method, further including: generating a command signal in response to

removing the work item from the enabled expansion bus schedule data structure;

where, generating a coherency signal utilizing an expansion bus host controller in

response to removing the work item from the enabled expansion bus schedule data

structure includes generating a status signal utilizing the expansion bus host controller

in response to generating the command signal (*see generally*, column 9, lines 17-24 and lines 35-60).

Ludtke does not expressly disclose all the features of dependent claims 2, 3, 12, 13, and 22.

Intel discloses where the enabled expansion bus schedule data structure comprises an asynchronous schedule including a plurality of queue heads and removing the work item from the enabled expansion bus schedule data structure includes unlinking a first queue head of the plurality of queue heads from the asynchronous schedule; and where the plurality of queue heads includes a second queue head, the second queue head includes a horizontal link pointer to the first queue head, and unlinking the first queue head from the asynchronous schedule includes modifying the horizontal link pointer of the second queue head (*see generally*, section 1.2.3; section 3.4.2; Fig. 4; and Fig. 11).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Intel with Ludtke. The suggestion or motivation for doing so would have been to increase system performance through use of the high transfer rates of the Universal Serial Bus (USB).

Therefore, it would have been obvious to combine Intel with Ludtke to obtain the invention as specified in claims 2-4, 12-14 and 22.

8.   Claims 2-4, 12-14 and 22 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Brief in view of *Universal Host Controller Interface (UHCI) Design

Guide*, Revision 1.1 by Intel ("Intel").

As discussed above with regard to the 35 USC 102(e) rejection, Brief discloses

all the features of claims 1, 11 and 21.   With regard to claims 4 and 14, Brief also

discloses the method, further including: generating a command signal in response to

removing the work item from the enabled expansion bus schedule data structure;

where, generating a coherency signal utilizing an expansion bus host controller in

response to removing the work item from the enabled expansion bus schedule data

structure includes generating a status signal utilizing the expansion bus host controller

in response to generating the command signal (*see generally*, column 8, lines 63-67 to

column 9, lines 1-31).

Brief does not expressly disclose all the features of dependent claims 2, 3, 12,

13, and 22.

Intel discloses where the enabled expansion bus schedule data structure

comprises an asynchronous schedule including a plurality of queue heads and

removing the work item from the enabled expansion bus schedule data structure

includes unlinking a first queue head of the plurality of queue heads from the

asynchronous schedule; and where the plurality of queue heads includes a second

queue head, the second queue head includes a horizontal link pointer to the first queue

head, and unlinking the first queue head from the asynchronous schedule includes

modifying the horizontal link pointer of the second queue head (*see generally*, section 1.2.3; section 3.4.2; Fig. 4; and Fig. 11).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Intel with Brief. The suggestion or motivation for doing so would have been to increase system performance through use of the high transfer rates of the Universal Serial Bus (USB).

Therefore, it would have been obvious to combine Intel with Brief to obtain the invention as specified in claims 2-4, 12-14, and 22.

9.   Claims 2-4, 12-14 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dussud in view of *Universal Host Controller Interface (UHCI) Design Guide*, Revision 1.1 by Intel ("Intel").

As discussed above with regard to the 35 USC 102(e) rejection, Dussud discloses all the features of claims 1, 11 and 21. With regard to claims 4 and 14, Dussud also discloses the method, further including: generating a command signal in response to removing the work item from the enabled expansion bus schedule data structure; where, generating a coherency signal utilizing an expansion bus host controller in response to removing the work item from the enabled expansion bus schedule data structure includes generating a status signal utilizing the expansion bus host controller in response to generating the command signal (*see generally*, column 8, lines 4-11 to column 9, lines 1-7). Also, *see generally*, column 4, lines 29-32 and column 5, lines 3-6.

Dussud does not expressly disclose all the features of dependent claims 2, 3, 12, 13, and 22.

Intel discloses where the enabled expansion bus schedule data structure comprises an asynchronous schedule including a plurality of queue heads and removing the work item from the enabled expansion bus schedule data structure includes unlinking a first queue head of the plurality of queue heads from the asynchronous schedule; and where the plurality of queue heads includes a second queue head, the second queue head includes a horizontal link pointer to the first queue head, and unlinking the first queue head from the asynchronous schedule includes modifying the horizontal link pointer of the second queue head (*see generally*, section 1.2.3; section 3.4.2; Fig. 4; and Fig. 11).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Intel with Dussud. The suggestion or motivation for doing so would have been to increase system performance through use of the high transfer rates of the Universal Serial Bus (USB).

Therefore, it would have been obvious to combine Intel with Dussud to obtain the invention as specified in claims 2-4, 12-14 and 22.

Response to Arguments

10.   Applicant's arguments (see pages 10-16 in Paper No. 7 filed July 8, 2004), with respect to the rejections of claims 1, 11, 21, 22, and 27 under 35 USC 102 and claims 2-10, 12-20, 23-26, and 28-30 have been fully considered and are persuasive.

Therefore, the rejections have been withdrawn. However, upon further consideration,

new grounds of rejection are made in view of U.S. Patent No. 6,763,391 to Ludtke, U.S.

Patent No. 6,205,501 to Brief, and U.S. Patent No. 6,804,762 to Dussud.

The Examiner is persuaded that U.S. Patent No. 4,755,939 to Watson does not

expressly disclose generating a coherency signal using an expansion bus host

controller and reclaiming the work item *whenever* the coherency signal is generated, as

claimed.

The Examiner is also persuaded that U.S. Patent No. 6,502,111 to Dussud does

not expressly disclose generating a coherency signal using an expansion bus host

controller, as claimed.

Furthermore, the Examiner is persuaded that the *Universal Controller Interface*

(UHCI) Design Guide does not expressly disclose where the status register including a

status signal bit to notify an expansion bus host controller driver that the work item may

be reclaimed, as claimed.

However, Ludtke, Brief, and the '762 patent to Dussud each disclose these

claimed features. Therefore, the Examiner cannot allow the claims.

Conclusion

11.   Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later
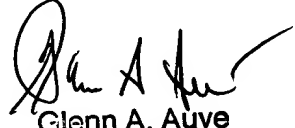
than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Donna K. Mason whose telephone number is (571) 272-

3629. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone

number for the organization where this application or proceeding is assigned is 703-

872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

DKM

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